## REMARKS

Claims 1-10, 12 are pending.

Claim 10 is rejected.

Claim 11 is canceled.

Claim 11 is objected to as depending from rejected Claim 10 but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim.

Claim 12 is added as Claim 11 rewritten to include the limitations of Claim 10 as suggested by the Examiner to put it into allowable form.

## I. EXAMINER INTERVIEW

The Applicant thanks the Examiner for the opportunity to discuss the present invention. Applicant had a telephone interview with the Examiner on April 13, 2005 to discuss the rejection of Claim 10. The Applicant noted that the cited prior art U.S. Patent No. 6,529,045 B1 to *Ye et al.* (hereafter "*Ye*") did not recite the limitation of Claim 10, specifically the limitations where the keeper circuitry reinforces a logic one on the dynamic node when the dynamic node is a logic one and the output is a logic one before transitioning to a logic zero. Further, the Applicant noted that the static circuitry of *Ye* is a simple inverter and does not latch the states of the dynamic node but rather follows the dynamic node. Only the combination of the static circuit, the inverter 303 and the keeper N2 provides latching of the logic one on the dynamic node. Since latching , according to the invention of *Ye*, requires the keeper circuit, the Applicant believes the keeper circuit of *Ye* is by definition not the static logic circuitry. The Examiner said he would call back on April 14, 2005 to discuss.

Applicant had a second telephone interview with the Examiner on April 14, 2005 to further discuss the rejection of Claim 10. Applicant appreciates the Examiner calling back to discuss the rejection of Claim 10. The Applicant noted that the static circuit in *Ye* cited by the Examiner is a simple inverter with only one output. To get the complementary output requires the Examiner to include inverter 303 as part of the static logic circuit. In this configuration, the static logic circuit provides no latching function. To provide any latching function, requires adding keeper N2 as part of the latching function. The present invention of Claim 10 has a static logic circuit for latching states of the dynamic node independent of the keeper as the keeper is a separate element. The Examiner said to send in the response and he would further evaluate. The Applicant informed the Examiner that he was adding a new Claim 12 which is Claim 11 rewritten in independent form while Applicant continues to argue that Claim 10 is distinctly different from the invention of *Ye*. Claim 11 has been canceled.

II. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claim 10 under *35 U.S.C. § 102(e)*, as being anticipated by U.S. Patent No. 6,529,045 B1 to *Ye et al.* (hereafter "*Ye*").

The Examiner states that Claim 10 is anticipated by *Ye* and cites FIG. 3 of *Ye* which is a prior art Domino logic circuit. See *Ye*, column 3, lines 36-38 and column 4, lines 40-42. The Examiner states that the dynamic logic circuit of *Ye* has an output (OUTPUT) and a complementary output (output of 303), the dynamic node (304), the precharge circuitry (NFET N1) coupled to the dynamic node 304 for precharging the dynamic node 304 to a logic one during a precharge of a clock signal (/CLK), and a logic tree (PULL-DOWN NMOS TREE) coupled to the dynamic node 304 for evaluating the dynamic node to a logic one or a logic zero in response to combinations of logic states of the plurality of logic inputs coupled to the logic tree during an evaluation cycle of the clock signal. However, the Examiner further states that the static logic circuitry for latching states of the dynamic node and holding the logic states during the precharge cycle of the clock signal is (STATIC CMOS) made of PFET 301 and NFET 302. PFET

301 and NFET 302 are configured as a simple CMOS inverter and as such does not latch logic states of the dynamic node and hold these states during the precharge cycle of the clock signal as claimed. The output of *Ye* inverter (STATIC CMOS) follows its input which is the dynamic node 304. Furthermore, the static logic circuitry of the present invention generates both the output and the complementary output. The logic inverter of *Ye* only generates one output. The Examiner then states that keeper circuit NFET N2 has a power supply terminal coupled to the power supply voltage (Vcc) and a keeper input (gate of NFET N2) coupled to the complementary output and a keeper output (drain of NFET N2) coupled to the dynamic node, wherein the keeper output reinforces a logic one state on the dynamic node only when the dynamic node evaluates to the logic one state and the output is the logic one state before transitioning to the logic zero state. First, the drain of NFET N2 is coupled to Vcc and not to the dynamic node, the source of NFET N2 is coupled to the dynamic node 304. If the keeper circuitry is NFET N2 as stated by the Examiner, then the keeper output does not reinforce a logic one state on the dynamic node only when the dynamic node evaluates to the logic one state and the output is the logic one state before transitioning to the logic zero state. When OUTPUT in FIG. 3 of *Ye* is a logic one, NFET N2 (by way of inverter 303) is turned OFF and thus decouples any current that would operate to reinforce a logic one at the dynamic node.

According to *Ye*, column 4, lines 40-42, "a further embodiment of the invention is shown in FIG. 3, which shows the circuit of FIG. 2 modified to use an inverter as the static CMOS circuit 201. In column 3 lines 47-52, *Ye* states (relative to FIG. 2); "when the inverted clock signal goes low, the level keeper circuit comprising n-channel transistor 204 and inverters 205 and 211 maintain a weakly held high voltage level at dynamic output node 207. The invention if *Ye* is a Domino logic circuit and as such does not latch logic states of the dynamic node. Further, the keeper circuitry of *Ye* does not operate like the keeper circuitry recited in Claim 10 of the present invention. The static circuitry recited in Claim 10 latch both logic states of the output 753 when the dynamic node is pre-charging. Likewise, the keeper circuitry of Claim 10 reinforces a logic one state on the dynamic node **only** when the dynamic node evaluates to a logic one state **and**

the output is the logic one state before transitioning to a logic zero state. The invention of Claim 10 can do this because the static logic circuitry and the keeper circuitry allow both the dynamic node and the output to both be a logic one prior to the evaluation mode. By definition, the circuit of *Ye* in FIG. 2 or FIG. 3 cannot have the dynamic node and the output node **both** at a logic one. Therefore, the Applicant believes that the rejection of Claim 10 under *35 U.S.C. § 102(e)*, as being anticipated by *Ye* is traversed by the above arguments.

III. OBJECTIONS

The Examiner objected to Claim 11 as depending from a rejected Claim 10. The Applicant has shown that Claim 10 is not anticipated by *Ye* and therefore the objection of Claim 11 is traversed. Claim 11 depends from Claim 10 which the Applicant has shown is distinctly different from the invention of *Ye*.

IV. CONCLUSION

Claims 1-9 are allowed.

The Applicant has traversed the rejection of Claim 10 under *35 U.S.C. § 102(e)*, as being anticipated by *Ye*.

The Applicant has traversed the objection of Claim 11 by the arguments sustaining the allowance of Claim 10.

The Applicants, therefore, respectfully assert that Claims 1-10, and new Claim 12 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Patent Agent and Attorney for Applicants

By: _____

Richard F. Frankeny
Reg. No. 47,573
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2872

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